



## SSC8626GN2

### N and P-Channel Enhancement Mode Power MOSFET

#### ➤ Features

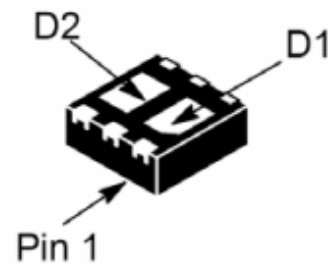
##### N-Channel

$V_{DS}$	$V_{GS}$	$R_{DS(ON)}$ Typ.	$I_D$
20V	$\pm 12V$	22m $\Omega$ @4.5V	7A
		27m $\Omega$ @2.5V	
		36m $\Omega$ @1.8V	

##### P-Channel

$V_{DS}$	$V_{GS}$	$R_{DS(ON)}$ Typ.	$I_D$
-20V	$\pm 12V$	63m $\Omega$ @-4.5V	-4A
		87m $\Omega$ @-2.5V	
		120m $\Omega$ @-1.8V	

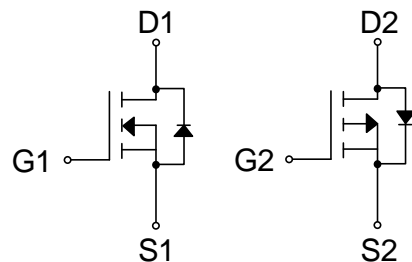
#### ➤ Pin configuration



DFN2020-6L

#### ➤ Description

SSC8626GN2 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.



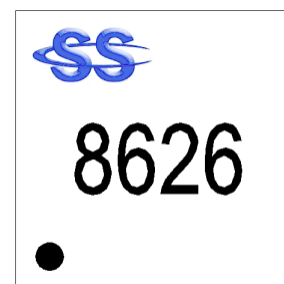
Pin Configuration (Top View)

#### ➤ Applications

- Signal
- CCFL Driver

#### ➤ Ordering Information

Device	Package	Shipping
SSC8626GN2	DFN2020-6L	3000/Reel



Marking



➤ **Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Symbol	Parameter	N-Channel	P-Channel	Unit
V <sub>DSS</sub>	Drain-to-Source Voltage	20	-20	V
V <sub>GSS</sub>	Gate-to-Source Voltage	± 12	± 12	V
I <sub>D</sub>	Continuous Drain Current <sup>d</sup>	7	-4	A
I <sub>DM</sub>	Pulsed Drain Current <sup>b</sup>	21	-12	A
P <sub>D</sub>	Power Dissipation <sup>c</sup>	1.9	1.9	W
T <sub>J</sub>	Operation junction temperature	-55~150		°C
T <sub>STG</sub>	Storage temperature range	-55~150		

➤ **Thermal Resistance Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>	65	$^{\circ}\text{C/W}$

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.



➤ **N-Channel Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

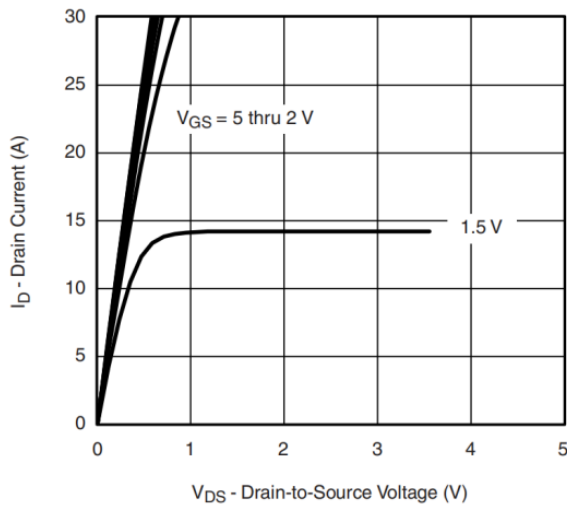
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.4	0.7	1.3	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 5A$		22	26	m $\Omega$
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 2.5V, I_D = 3.5A$		27	35	m $\Omega$
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 1.8V, I_D = 2.8A$		36	55	m $\Omega$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16V, V_{GS} = 0V$			1	$\mu A$
Gate-Source Leak Current	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 100$	nA
Forward Transconductance	$G_{FS}$	$V_{DS}=5V, I_D=7A$		7		S
Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = 1.1A$		0.8	1.3	V
Input Capacitance	$C_{ISS}$	$V_{DS} = 10V, V_{GS} = 0V,$ $f = 1MHz$		406		pF
Output Capacitance	$C_{OSS}$			68		
Reverse Transfer Capacitance	$C_{RSS}$			57		
Total Gate Charge	$Q_G$	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_D = 7A$		11		nC
Gate to Source Charge	$Q_{GS}$			1		
Gate to Drain Charge	$Q_{GD}$			1.5		
Turn-on Delay Time	$T_{D(ON)}$	$V_{GS} = 4.5V, V_{DS} = 10V,$ $R_G = 3\Omega, I_D = 7A$		3		ns
Rise Time	$T_r$			7.5		
Turn-off Delay Time	$T_{D(OFF)}$			20		
Fall Time	$T_f$			6		

**➤ P-Channel Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

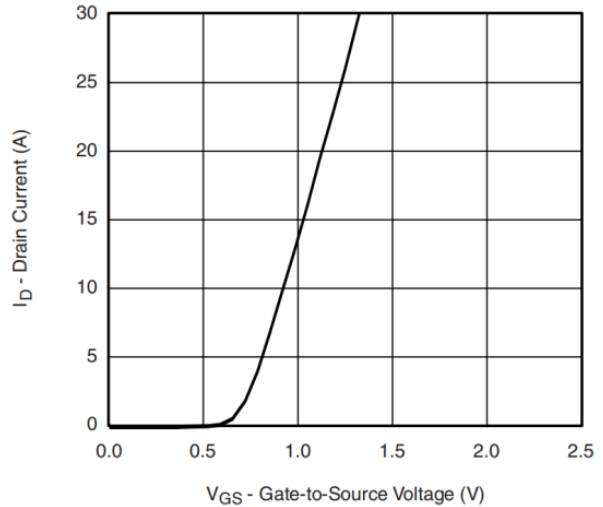
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.5	-0.7	-1.2	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -2.8A$		63	80	mΩ
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -2.5V, I_D = -2.3A$		87	110	mΩ
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -1.8V, I_D = -0.5A$		120	200	mΩ
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16V, V_{GS} = 0V$			-1	μA
Gate-Source Leak Current	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			±100	nA
Forward Transconductance	$G_{FS}$	$V_{DS} = -5V, I_D = -4A$		4		S
Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = -0.9A$		-0.7	-1.3	V
Input Capacitance	$C_{ISS}$	$V_{DS} = -10V, V_{GS} = 0V,$ $f = 1MHz$		730		pF
Output Capacitance	$C_{OSS}$			72		
Reverse Transfer Capacitance	$C_{RSS}$			60		
Total Gate Charge	$Q_G$	$V_{GS} = -4.5V, V_{DS} = -10V,$ $I_D = -4A$		8		nC
Gate to Source Charge	$Q_{GS}$			1		
Gate to Drain Charge	$Q_{GD}$			2		
Turn-on Delay Time	$T_{D(ON)}$	$V_{GS} = -4.5V, V_{DS} = -10V,$ $R_G = 3\Omega, I_D = -4A$		12		ns
Rise Time	$T_r$			11		
Turn-off Delay Time	$T_{D(OFF)}$			40		
Fall Time	$T_f$			17		



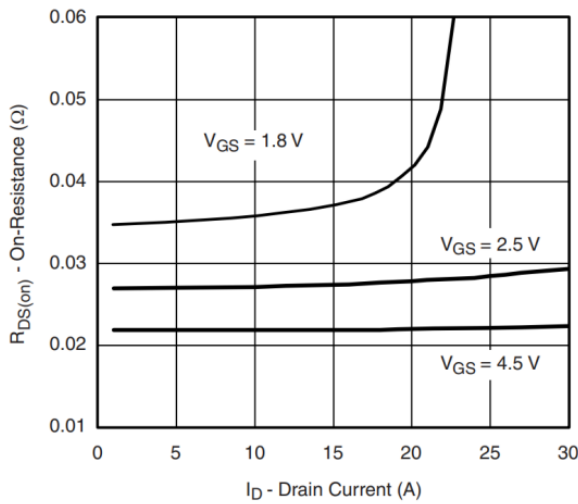
## ➤ N-Channel Typical Performance Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)



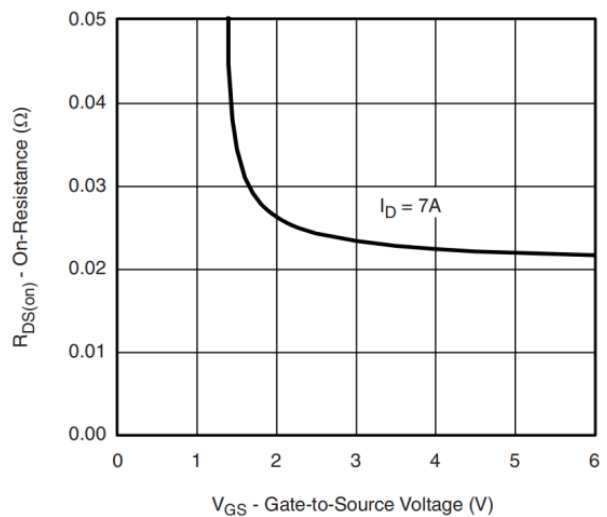
**Output Characteristics**



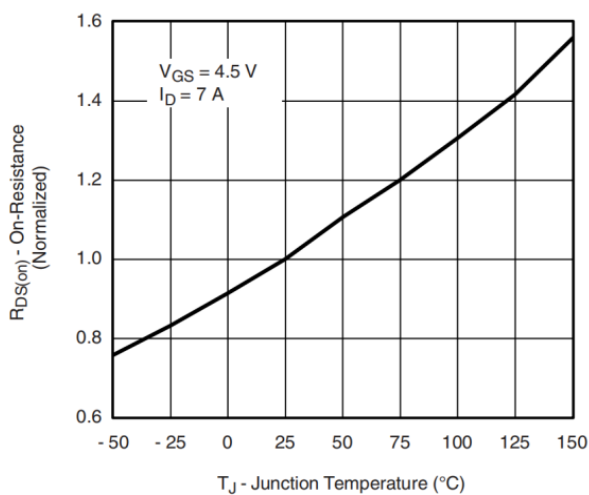
**Transfer Characteristics**



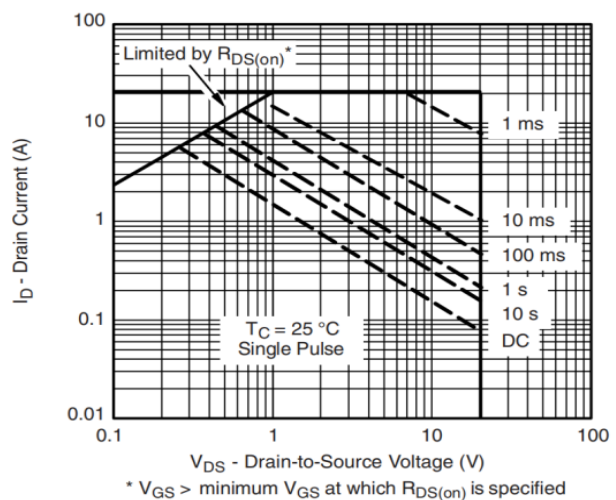
**On-Resistance vs. Drain Current**



**On-Resistance vs. Gate-to-Source Voltage**



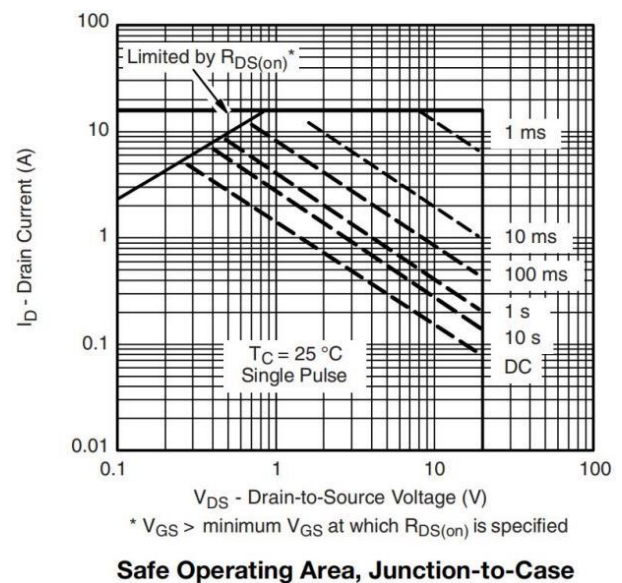
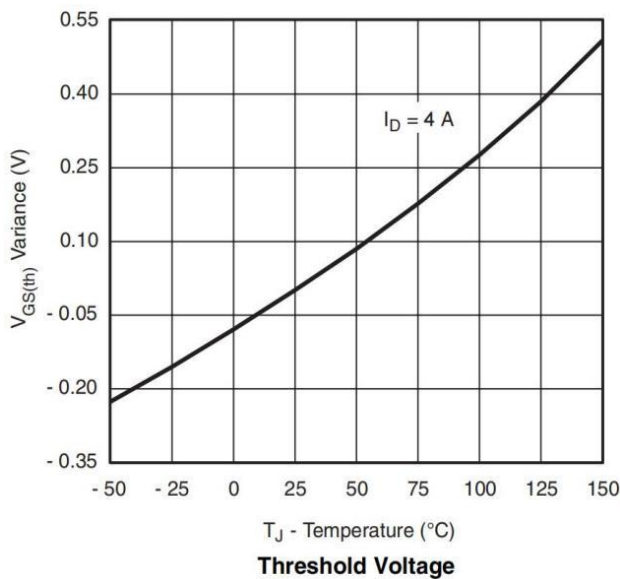
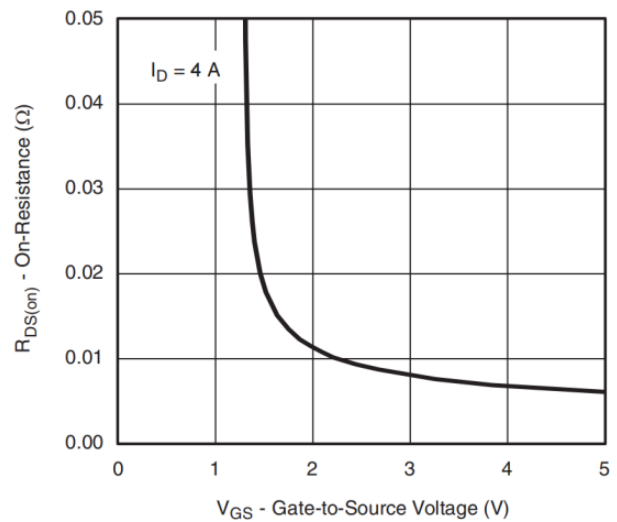
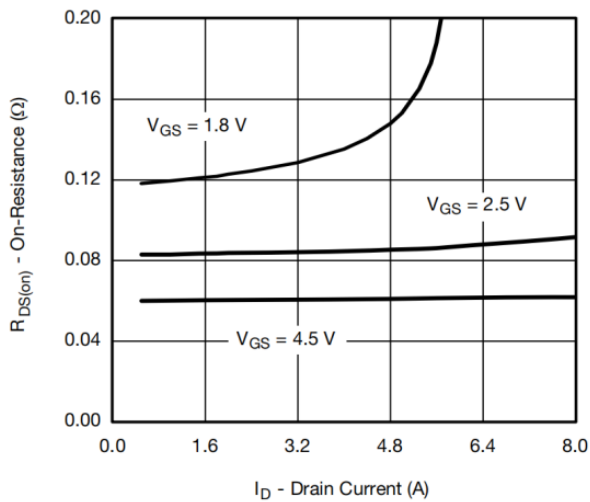
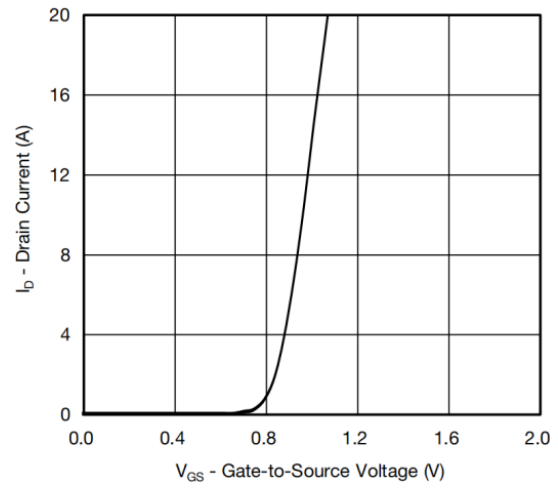
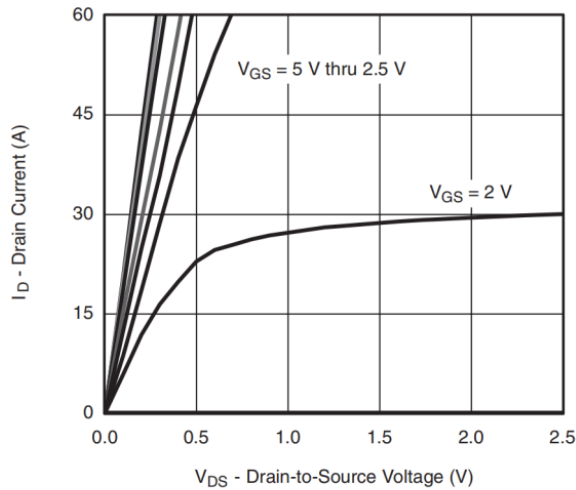
**On-Resistance vs. Junction Temperature**



**Safe Operating Area, Junction-to-Case**

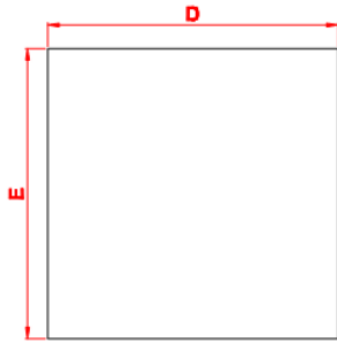


## ➤ P-Channel Typical Performance Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

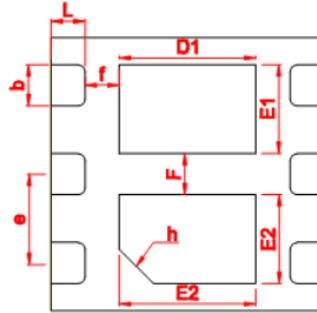




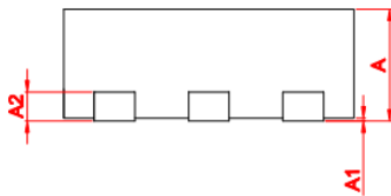
## ➤ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
* A1	0.000	0.020	0.050
* b	0.275	0.300	0.325
* A2	0.190	0.210	0.230
* D	1.900	2.000	2.100
* E	1.900	2.000	2.100
* E1	0.570	0.620	0.670
* E2	0.570	0.620	0.670
* D1	0.950	1.000	1.050
* D2	0.950	1.000	1.050
* e	0.600	0.650	0.700
h	0.300	0.350	0.400
* L	0.200	0.250	0.300
* F	0.250	0.300	0.350
* f	0.200	0.250	0.300



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